ABSTRACT OF THE DISCLOSURE

A method determines a plurality of clock delay values. Each delay value is associated with a delay element on a clock line leading to a clock sink in a synchronous circuit. The method determines an initial set of delay values and executes an optimization algorithm, beginning with the initial set of delay values, to arrive at a set of delay values that at least approximately meets an criteria while satisfying timing constraints associated with selected pairs of logically connected clock sinks. In a preferred form, the optimization algorithm is a genetic algorithm or a gradient descent algorithm. The genetic algorithm involves selecting parent sets of delay values, crossing over so as to produce a child set of delay values, mutating the child set of delay values, evaluating how well the child set of delay values meets the criteria, and conditionally discarding the child set on the basis of the evaluating step. The gradient descent algorithm involves perturbing the initial set of delay values, evaluating how well the perturbed set of delay values meets the criteria, and conditionally discarding the perturbed set on the basis of the evaluating step. If the perturbed set is not discarded, then the gradient descent algorithm adjusts the values of the perturbed set in the same direction relative to the corresponding values in the initial set.